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Title: SEMICONDUCTOR CHIP MODULE

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- ☒ 9 sheets of formal drawings
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19	–	20	=	0	x	0.00	=	$0.00
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Serial or Patent No.: Docket No.:
Filed or Issued:
For: SEMICONDUCTOR CHIP MODULE

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As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9 (c) for purposes of paying reduced fees under section 41 (a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention entitled SEMICONDUCTOR CHIP MODULE described in

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Ming-Tung SHEN

NAME OF INVENTOR NAME OF INVENTOR NAME OF INVENTOR

Signature of Inventor Signature of Inventor Signature of Inventor

Sep. 16, 1999

Date Date Date

SEMICONDUCTOR CHIP MODULE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a semiconductor chip module, more particularly to semiconductor chip modules that can be stacked one on top of the other in a fully automated manner.

2. Description of the Related Art

In this age of computer technology, there is an ever-growing need to increase the speed and functionality of computers, thereby resulting in a corresponding need to increase the memory capacity. However, due to limitations in the size of a computer main board, the number of on-board memory devices that can be installed is severely limited. There is thus a need to develop a memory device having a capacity that can be expanded without incurring a substantial increase in board penalty.

In U.S. Patent No. 4,996,587, there is disclosed an integrated semiconductor chip package that includes a plurality of chip carriers arranged in a stack, and a plurality of semiconductor chips mounted on the chip carriers. However, due to the need for S-shaped connector clips mounted on the chip carriers to establish electrical connection among the semiconductor chips, the integrated semiconductor chip package according to the aforesaid U.S. patent cannot

be manufactured in a fully automated manner, thereby resulting in increased production costs.

SUMMARY OF THE INVENTION

Therefore, the object of the present invention is to provide semiconductor chip modules that can be stacked one on top of the other in a fully automated manner.

According to one aspect of the invention, a semiconductor chip module comprises:

a chip-mounting member having opposite first and second surfaces, a set of circuit traces, and a plurality of plated through holes that extend through the first and second surfaces and that are connected to the circuit traces;

a semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;

a dielectric tape member for bonding adhesively the semiconductor chip on the chip-mounting member;

a conductor unit for connecting electrically the contact pads of the semiconductor chip and the circuit traces; and

a plurality of solder balls disposed on one of the first and second surfaces of the chip-mounting member, each of the solder balls being aligned with and being connected to a respective one of the plated through holes in the chip-mounting member.

According to another aspect of the invention, a semiconductor chip module stack comprises upper and lower semiconductor chip modules, each including:

a chip-mounting member having upper and lower surfaces, a set of circuit traces, and a plurality of plated through holes that extend through the upper and lower surfaces and that are connected to the circuit traces;

a semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;

a dielectric tape member for bonding adhesively the semiconductor chip on the chip-mounting member;

a conductor unit for connecting electrically the contact pads of the semiconductor chip and the circuit traces; and

a plurality of solder balls disposed on the lower surface of the chip-mounting member, each of the solder balls being aligned with and being connected to a respective one of the plated through holes in the chip-mounting member.

The solder balls of the upper semiconductor chip module are aligned with and are connected to the plated through holes in the chip-mounting member of the lower semiconductor chip module at the upper surface of the latter.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the present invention will become apparent in the following detailed description of the preferred embodiments with reference to the accompanying drawings, of which:

Figure 1 is a fragmentary schematic partly sectional view of the first preferred embodiment of a semiconductor chip module according to the present invention;

Figure 2 is a fragmentary perspective view of a chip-mounting member of the first preferred embodiment;

Figure 3 is a perspective view illustrating a semiconductor chip of the first preferred embodiment;

Figure 4 is a perspective view illustrating a dielectric tape member of the first preferred embodiment;

Figure 5 is a fragmentary schematic partly sectional view illustrating how a plurality of the semiconductor chip modules of the first preferred embodiment can be interconnected to form a stack;

Figure 6 is a fragmentary schematic partly sectional view of the second preferred embodiment of a semiconductor chip module according to the present invention;

Figure 7 is a fragmentary schematic partly sectional view illustrating how a plurality of the semiconductor

chip modules of the second preferred embodiment can be interconnected to form a stack;

Figure 8 is a fragmentary schematic partly sectional view of the third preferred embodiment of a semiconductor chip module according to the present invention;

Figure 9 is a fragmentary schematic partly sectional view illustrating how a plurality of the semiconductor chip modules of the third preferred embodiment can be interconnected to form a stack;

Figure 10 is a fragmentary schematic partly sectional view of the fourth preferred embodiment of a semiconductor chip module according to the present invention;

Figure 11 is a fragmentary schematic partly sectional view illustrating how a plurality of the semiconductor chip modules of the fourth preferred embodiment can be interconnected to form a stack; and

Figure 12 is a fragmentary schematic partly sectional view of the fifth preferred embodiment of a semiconductor chip module according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before the present invention is described in greater detail, it should be noted that like elements are denoted by the same reference numerals throughout the disclosure.

Referring to Figure 1, the first preferred embodiment of a semiconductor chip module according to the present invention is shown to comprise a chip-mounting member 1, at least two semiconductor chips 2, and a plurality of solder balls 3.

In this embodiment, the chip-mounting member 1 is a board body having opposite first and second chip mounting surfaces 10, 11 that are respectively formed with circuit traces 12 (see Figure 2). The chip-mounting member 1 is further formed with a plurality of plated through holes 14 that extend through the first and second chip mounting surfaces 10, 11 and that are connected electrically to the circuit traces 12 on the surfaces 10, 11.

Each of the semiconductor chips 2 has a pad mounting surface 20 with a plurality of contact pads 21 provided thereon (see Figure 3). The pad mounting surface 20 of each of the semiconductor chips 2 is bonded adhesively on one of the first and second chip mounting surfaces 10, 11 via a dielectric tape member 4. Particularly, the dielectric tape member 4 has a first adhesive surface adhered onto the pad mounting surface 20 of the semiconductor chip 2, and an opposite second adhesive surface adhered onto the first or second chip mounting surface 10, 11. The dielectric tape member 4 is formed with a plurality of holes 40 at positions registered with the contact pads 21 of the semiconductor chip 2

(see Figure 4). Conductive contact balls 5 are received in the holes 40 to establish electrical connection between the contact pads 21 of the semiconductor chip 2 and the circuit traces 12 on the first or second chip mounting surface 10, 11. Preferably, each semiconductor chip 2 has a peripheral portion that is provided with an epoxy resin layer 23 to strengthen bonding of the semiconductor chip 2 with the first or second chip mounting surface 10, 11. Moreover, each semiconductor chip 2 has a heat dissipating surface that is opposite to the pad mounting surface and that has a heat dissipating plate 24 secured thereon for heat dissipating and chip protection purposes.

Each of the solder balls 3 (only two are shown in Figure 1) is made from tin and is disposed on the second chip mounting surface 11 of the chip-mounting member 1. Each of the solder balls 3 is aligned with and is connected to a respective one of the plated through holes 14 in the chip-mounting member 1. Thus, electrical connection between the solder balls 3 and the contact pads 21 of the semiconductor chips 2 can be established via the circuit traces 12 on the surfaces 10, 11 of the chip-mounting member 1.

While Figure 1 shows only one semiconductor chip 2 mounted on each of the surfaces 10, 11 of the chip-mounting member 1, it should be clear to one skilled in the art that two or more semiconductor chips 2 may

be mounted on each of the surfaces 10, 11.

Referring to Figure 5, two or more semiconductor chip modules of the first preferred embodiment can be interconnected to form a semiconductor chip module stack. As shown, the solder balls 3 on an upper one of the semiconductor chip modules are aligned with and are connected to the plated through holes 14 in the chip-mounting member 1 of a lower one of the semiconductor chip modules at the first chip mounting surface 10 of the latter. The solder balls 3 of a lowermost one of the semiconductor chip modules in the semiconductor chip module stack can be mounted on a printed circuit board (not shown) for establishing electrical connection with circuit traces on the latter.

Figure 6 illustrates the second preferred embodiment of a semiconductor chip module according to the present invention. As shown, the chip-mounting member 1 is a three-layer board body having opposite first and second chip mounting surfaces 10, 11 that are respectively formed with circuit traces similar to those shown in Figure 2. The chip-mounting member 1 is further formed with a plurality of plated through holes 14 that extend through the first and second chip mounting surfaces 10, 12 and that are connected electrically to the circuit traces on the surfaces 10, 11. Each of the surfaces 10, 11 is formed with at least

one chip receiving cavity 13 having an open end and a closed end opposite to the open end. Each of the semiconductor chips 2 has a pad mounting surface 20 with a plurality of contact pads 21 provided thereon, and an opposite chip fixing surface. Each of the semiconductor chips 2 is received in a respective one of the chip receiving cavities 13 in the chip-mounting member 1 with the pad mounting surface 20 being accessible from the first or second chip mounting surface 10, 11 via the open end of the respective one of the chip receiving cavities 13. The chip fixing surface of each of the semiconductor chips 2 is bonded adhesively on the closed end of the respective one of the chip receiving cavities 13 via a dielectric tape member 4a. Particularly, the dielectric tape member 4a has a first adhesive surface adhered onto the chip fixing surface of the semiconductor chip 2, and an opposite second adhesive surface adhered onto the closed end of the respective one of the chip receiving cavities 13. In addition, wires 22 interconnect the contact pads 21 of the semiconductor chip 2 and the circuit traces on the first or second chip mounting surface 10, 11. Preferably, an encapsulation layer 6, made of epoxy resin, is provided on each of the first and second chip mounting surfaces 10, 11 to enclose the pad mounting surface 20 of each semiconductor chip 2 and the wires 22 that are connected to the semiconductor

chip 2 for protection purposes. Like the previous embodiment, each of the solder balls 3 is disposed on the second chip mounting surface 11 of the chip-mounting member 1, and is aligned with and is connected to a respective one of the plated through holes 14 in the chip-mounting member 1. Thus, electrical connection between the solder balls 3 and the contact pads 21 of the semiconductor chips 2 can be established via the wires 22 and the circuit traces on the surfaces 10, 11 of the chip-mounting member 1.

Referring to Figure 7, two or more semiconductor chip modules of the second preferred embodiment can be interconnected to form a semiconductor chip module stack. As shown, the solder balls 3 on an upper one of the semiconductor chip modules are aligned with and are connected to the plated through holes 14 in the chip-mounting member 1 of a lower one of the semiconductor chip modules at the first chip mounting surface 10 of the latter. The solder balls 3 of a lowermost one of the semiconductor chip modules in the semiconductor chip module stack can be mounted on a printed circuit board (not shown) for establishing electrical connection with circuit traces on the latter.

Figure 8 illustrates the third preferred embodiment of a semiconductor chip module according to the present invention. As shown, the chip-mounting member 1 is a

three-layer board body having opposite first and second chip mounting surfaces 10, 11 formed with at least one chip receiving cavity 13a having an open end and a closed end opposite to the open end. The chip-mounting member 1 is further formed with a plurality of plated through holes 14 that extend through the surfaces 10, 12. The first and second chip mounting surfaces 10, 11 and the closed end of each chip receiving cavity 13a are respectively formed with circuit traces similar to those shown in Figure 2 and connected electrically to the plated through holes 14. Each of the chip receiving cavities 13 receives two semiconductor chips 2a, 2b therein. Each of the semiconductor chips 2a, 2b has a pad mounting surface 20 with a plurality of contact pads 21 provided thereon, and an opposite chip fixing surface. The pad mounting surface 20 of each of the semiconductor chips 2a is bonded adhesively on the closed end of the respective one of the chip receiving cavities 13a via a dielectric tape layer 4. Particularly, the dielectric tape layer 4 has a first adhesive surface adhered onto the pad mounting surface 20 of the semiconductor chip 2a, and an opposite second adhesive surface adhered onto the closed end of the respective one of the chip receiving cavities 13a. Like the first preferred embodiment, the dielectric tape layer 4 is formed with a plurality of holes 40 at positions registered with the contact pads 21 of the

semiconductor chip 2a. Conductive contact balls 5 are received in the holes 40 to establish electrical connection between the contact pads 21 of the semiconductor chip 2a and the circuit traces on the closed end of the respective one of the chip receiving cavities 13a. Each of the semiconductor chips 2b is received in the respective one of the chip receiving cavities 13a with the pad mounting surface 20 thereof being accessible from the first or second chip mounting surface 10, 11 via the open end of the respective one of the chip receiving cavities 13a. The chip fixing surface of each of the semiconductor chips 2b is bonded adhesively on the chip fixing surface of the semiconductor chip 2a that is disposed in the same one of the chip receiving cavities 13a via another dielectric tape layer 4a. Particularly, the dielectric tape layer 4a has a first adhesive surface adhered onto the chip fixing surface of the semiconductor chip 2b, and an opposite second adhesive surface adhered onto the chip fixing surface of the semiconductor chip 2a. In addition, like the second preferred embodiment, wires 22 interconnect the contact pads 21 of the semiconductor chip 2b and the circuit traces on the first or second chip mounting surface 10, 11. Moreover, an encapsulation layer 6, made of epoxy resin, is provided on each of the surfaces 10, 11 of the chip-mounting member 1 to enclose the pad mounting

surface 20 of each semiconductor chip 2b and the wires 22 that are connected to the semiconductor chip 2b for protection purposes. As with the previous embodiments, each of the solder balls 3 is disposed on the second chip mounting surface 11, and is aligned with and is connected to a respective one of the plated through holes 14 in the chip-mounting member 1. Thus, electrical connection between the solder balls 3 and the contact pads 21 of the semiconductor chips 2a can be established via the circuit traces on the closed ends of the chip receiving cavities 13a, while electrical connection between the solder balls 3 and the contact pads 21 of the semiconductor chips 2b can be established via the wires 22 and the circuit traces on the surfaces 10, 11 of the chip-mounting member 1.

Referring to Figure 9, two or more semiconductor chip modules of the third preferred embodiment can be interconnected to form a semiconductor chip module stack. As shown, the solder balls 3 on an upper one of the semiconductor chip modules are aligned with and are connected to the plated through holes 14 in the chip-mounting member 1 of a lower one of the semiconductor chip modules at the first chip mounting surface 10 of the latter. The solder balls 3 of a lowermost one of the semiconductor chip modules in the semiconductor chip module stack can be mounted on a printed circuit board (not shown) for establishing

electrical connection with circuit traces on the latter.

Referring to Figure 10, the fourth preferred embodiment of a a semiconductor chip module according to the present invention is shown to comprise first and second chip-mounting members 1a, 1b, a first semiconductor chip 2a, a second semiconductor chip 2b, a plurality of first solder balls 3a, and a plurality of second solder balls 3b.

In this embodiment, the first chip-mounting member 1a is a board body having an upper chip mounting surface 15a and a lower circuit layout surface 16a formed with circuit traces similar to those shown in Figure 2. The first chip-mounting member 1a is further formed with an opening 17a and a plurality of plated through holes 14a that extend through the surfaces 15a, 16a and that are connected electrically to the circuit traces on the circuit layout surface 16a. The first semiconductor chip 2a has a pad mounting surface 20a with a plurality of contact pads 21a provided thereon. The pad mounting surface 20a is bonded adhesively on the chip mounting surface 15a using a dielectric tape member 7. Particularly, the dielectric tape member 7 has a first adhesive surface adhered onto the pad mounting surface 20a, and an opposite second adhesive surface adhered onto the chip mounting surface 15a. The dielectric tape member 7 is formed with an opening 70 that is registered

with the opening 17a such that the contact pads 21a are accessible from the circuit layout surface 16a via the openings 17a, 70. Wires 22a interconnect the contact pads 21a and the circuit traces on the circuit layout surface 16a. Preferably, a peripheral portion of the first semiconductor chip 2a is provided with an epoxy resin layer 23a to strengthen bonding of the first semiconductor chip 2a with the chip mounting surface 15a. Moreover, the first semiconductor chip 2a has a heat dissipating surface that is opposite to the pad mounting surface 20a and that has a heat dissipating plate 24a secured thereon for heat dissipating and chip protection purposes. In addition, an encapsulation layer 6a made of epoxy resin is provided on the circuit layout surface 16a to enclose the pad mounting surface 20a and the wires 22a for protection purposes. Each of the first solder balls 3a (only two are shown in Figure 10) is made from tin and is disposed on the circuit layout surface 16a. Each of the first solder balls 3a is aligned with and is connected to a respective one of the plated through holes 14a in the first chip-mounting member 1a. Thus, electrical connection between the first solder balls 3a and the contact pads 21a of the first semiconductor chip 2a can be established via the circuit traces on the circuit layout surface 16a and the wires 22a.

Unlike the first chip-mounting member 1a, the second chip-mounting member 1b is a board body having a lower chip mounting surface 15b and an upper circuit layout surface 16b formed with circuit traces similar to those shown in Figure 2. The second chip-mounting member 1b is further formed with an opening 17b and a plurality of plated through holes 14b that extend through the surfaces 15b, 16b and that are connected electrically to the circuit traces on the circuit layout surface 16b. The second semiconductor chip 2b has a pad mounting surface 20b with a plurality of contact pads 21b provided thereon. The pad mounting surface 20b is bonded adhesively on the chip mounting surface 15b using a dielectric tape member 8. Particularly, the dielectric tape member 8 has a first adhesive surface adhered onto the pad mounting surface 20b, and an opposite second adhesive surface adhered onto the chip mounting surface 15b. The dielectric tape member 8 is formed with an opening 80 that is registered with the opening 17b such that the contact pads 21b are accessible from the circuit layout surface 16b via the openings 17b, 80. Wires 22b interconnect the contact pads 21b and the circuit traces on the circuit layout surface 16b. Like the first semiconductor chip 2a, a peripheral portion of the second semiconductor chip 2b is provided with an epoxy resin layer 23b to strengthen bonding of the second semiconductor chip 2b with the

chip mounting surface 15b. Moreover, the second semiconductor chip 2b has a heat dissipating surface that is opposite to the pad mounting surface 20b and that has a heat dissipating plate 24b secured thereon for heat dissipating and chip protection purposes. In addition, an encapsulation layer 6b made of epoxy resin is provided on the circuit layout surface 16b to enclose the pad mounting surface 20b and the wires 22b for protection purposes. Each of the second solder balls 3b (only two are shown in Figure 10) is made from tin and is disposed on the chip mounting surface 15b. Each of the second solder balls 3b is aligned with and is connected to a respective one of the plated through holes 14b in the second chip-mounting member 1b. Thus, electrical connection between the second solder balls 3b and the contact pads 21b of the second semiconductor chip 2b can be established via the circuit traces on the circuit layout surface 16b and the wires 22b.

In this embodiment, the second chip-mounting member 1b is disposed below the first chip-mounting member 1a, and each of the first solder balls 3a on the circuit layout surface 16a of the first chip-mounting member 1a is aligned with and is connected to a respective one of the plated through holes 14b at the circuit layout surface 16a of the second chip-mounting member 1b.

Referring to Figure 11, two or more semiconductor chip modules of the fourth preferred embodiment can be

interconnected to form a semiconductor chip module stack. As shown, the second solder balls 3b on an upper one of the semiconductor chip modules are aligned with and are connected to the plated through holes 14a at the chip mounting surface 15a of the first chip-mounting member 1a of a lower one of the semiconductor chip modules. The second solder balls 3b of a lowermost one of the semiconductor chip modules in the semiconductor chip module stack can be mounted on a printed circuit board (not shown) for establishing electrical connection with circuit traces on the latter.

Figure 12 illustrates the fifth preferred embodiment of a semiconductor chip module according to the present invention. In contrast with the fourth preferred embodiment, each of the first and second chip-mounting members 1a, 1b has at least two first and second semiconductor chips 2a, 2b mounted respectively thereon.

It has thus been shown that the semiconductor chip module of this invention does not require the use of connector clips to establish electrical connection with other semiconductor chip modules. The semiconductor chip module can be manufactured in a fully automated manner to result in lower production costs. When the semiconductor chips are memory chips, a significant increase in memory capacity is possible

without incurring a significant increase in board penalty. The object of the present invention is thus met.

While the present invention has been described in connection with what is considered the most practical and preferred embodiments, it is understood that this invention is not limited to the disclosed embodiments but is intended to cover various arrangements included within the spirit and scope of the broadest interpretation so as to encompass all such modifications and equivalent arrangements.

I CLAIM:

1. A semiconductor chip module comprising:

a chip-mounting member having opposite first and second surfaces, a set of first circuit traces, and a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces;

a first semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;

a first dielectric tape member for bonding adhesively said first semiconductor chip on said chip-mounting member;

a first conductor unit for connecting electrically said contact pads of said first semiconductor chip and said first circuit traces; and

a plurality of solder balls disposed on one of said first and second surfaces of said chip-mounting member, each of said solder balls being aligned with and being connected to a respective one of said plated through holes in said chip-mounting member.

2. The semiconductor chip module as claimed in Claim 1, wherein:

said first circuit traces and said first semiconductor chip are disposed on a same one of said first and second surfaces of said chip-mounting member;

said first dielectric tape member bonds adhesively said pad mounting surface of said first semiconductor chip on said same one of said first and second surfaces of said chip-mounting member, and is formed with a plurality of holes at positions registered with said contact pads of said first semiconductor chip; and

said first conductor unit includes a plurality of conductive contact balls that are received in said holes in said first dielectric tape member to establish electrical connection between said contact pads of said first semiconductor chip and said first circuit traces.

3. The semiconductor chip module as claimed in Claim 2, wherein said chip-mounting member further has a set of second circuit traces accessible from the other one of said first and second surfaces opposite to said first circuit traces and connected to said plated through holes, said semiconductor chip module further comprising:

a second semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;

a second dielectric tape member for bonding adhesively said second semiconductor chip on said chip-mounting member; and

a second conductor unit for connecting electrically said contact pads of said second semiconductor chip and said second circuit traces.

4. The semiconductor chip module as claimed in Claim 3, wherein:

said second dielectric tape member bonds adhesively said pad mounting surface of said second semiconductor chip on the other one of said first and second surfaces of said chip-mounting member, and is formed with a plurality of holes at positions registered with said contact pads of said second semiconductor chip; and

said second conductor unit includes a plurality of conductive contact balls that are received in said holes in said second dielectric tape member to establish electrical connection between said contact pads of said second semiconductor chip and said second circuit traces.

5. The semiconductor chip module as claimed in Claim 2, wherein said first semiconductor chip has a peripheral portion that is provided with an epoxy resin layer to strengthen bonding of said first semiconductor chip with said same one of said first and second surfaces of said chip-mounting member.

6. The semiconductor chip module as claimed in Claim 2, wherein said first semiconductor chip has a heat dissipating surface that is opposite to said pad mounting surface and that has a heat dissipating plate secured thereon.

7. The semiconductor chip module as claimed in Claim 1, wherein:

said chip-mounting member has a first chip receiving cavity formed in one of said first and second surfaces thereof, said first chip receiving cavity having an open end and a closed end opposite to said open end, said first circuit traces and said first chip receiving cavity being provided on a same one of said first and second surfaces of said chip-mounting member;

said first semiconductor chip is received in said first chip receiving cavity with said pad mounting surface thereof being accessible from said same one of said first and second surfaces of said chip-mounting member via said open end of said first chip receiving cavity; and

said first conductor unit includes a plurality of conductive wires that interconnect said contact pads of said first semiconductor chip and said first circuit traces.

8. The semiconductor chip module as claimed in Claim 7, wherein said first semiconductor chip has a chip fixing surface opposite to said pad mounting surface, said first dielectric tape member bonding adhesively said chip fixing surface of said first semiconductor chip on said closed end of said first chip receiving cavity.

9. The semiconductor chip module as claimed in Claim 7, wherein said chip-mounting member further has a set of second circuit traces accessible from the other one

of said first and second surfaces opposite to said first circuit traces and connected to said plated through holes, said semiconductor chip module further comprising:

a second semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;

a second dielectric tape member for bonding adhesively said second semiconductor chip on said chip-mounting member; and

a second conductor unit for connecting electrically said contact pads of said second semiconductor chip and said second circuit traces.

10. The semiconductor chip module as claimed in Claim 9, wherein:

said chip-mounting member has a second chip receiving cavity formed in the other one of said first and second surfaces thereof, said second chip receiving cavity having an open end and a closed end opposite to said open end;

said second semiconductor chip is received in said second chip receiving cavity with said pad mounting surface thereof being accessible from the other one of said first and second surfaces of said chip-mounting member via said open end of said second chip receiving cavity; and

said second conductor unit includes a plurality of conductive wires that interconnect said contact pads of said second semiconductor chip and said second circuit traces.

11. The semiconductor chip module as claimed in Claim 10, wherein said second semiconductor chip has a chip fixing surface opposite to said pad mounting surface, said second dielectric tape member bonding adhesively said chip fixing surface of said second semiconductor chip on said closed end of said second chip receiving cavity.

12. The semiconductor chip module as claimed in Claim 7, further comprising an encapsulation layer provided on said same one of said first and second surfaces of said chip-mounting member to enclose said pad mounting surface of said first semiconductor chip and said first conductor unit.

13. The semiconductor chip module as claimed in Claim 7, wherein said closed end of said first chip receiving cavity is formed with a set of second circuit traces that are connected to said plated through holes, said first semiconductor chip having a chip fixing surface opposite to said pad mounting surface, said semiconductor chip module further comprising:

a second semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon, and a chip fixing surface opposite to said pad

mounting surface, said second semiconductor chip being received in said first chip receiving cavity between said first semiconductor chip and said closed end of said first chip receiving cavity;

said first dielectric tape member including a first dielectric tape layer for bonding together said chip fixing surfaces of said first and second semiconductor chips, and a second dielectric tape layer for bonding adhesively said pad mounting surface of said second semiconductor chip on said closed end of said first chip receiving cavity, said second dielectric tape layer being formed with a plurality of holes at positions registered with said contact pads of said second semiconductor chip; and

a second conductor unit including a plurality of conductive contact balls that are received in said holes in said second dielectric tape layer to establish electrical connection between said contact pads of said second semiconductor chip and said second circuit traces.

14. The semiconductor chip module as claimed in Claim 13, wherein said chip-mounting member further has a set of third circuit traces accessible from the other one of said first and second surfaces opposite to said first circuit traces and connected to said plated through holes, said semiconductor chip module further comprising:

a third semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;

a third dielectric tape member for bonding adhesively said third semiconductor chip on said chip-mounting member; and

a third conductor unit for connecting electrically said contact pads of said third semiconductor chip and said third circuit traces.

15. The semiconductor chip module as claimed in Claim 1, wherein said first circuit traces are disposed on one of said first and second surfaces of said chip-mounting member, said first dielectric tape member bonding adhesively said pad mounting surface of said first semiconductor chip on the other one of said first and second surfaces of said chip-mounting member, said chip-mounting member being formed with a first opening that extends through said first and second surfaces thereof, said first dielectric tape member being formed with a second opening that is registered with said first opening for access to said contact pads of said first semiconductor chip, said first conductor unit including a plurality of wires that interconnect said contact pads of said first semiconductor chip and said first circuit traces.

16. The semiconductor chip module as claimed in Claim 15, wherein said first semiconductor chip has a

peripheral portion that is provided with an epoxy resin layer to strengthen bonding of said first semiconductor chip with the other one of said first and second surfaces of said chip-mounting member.

17. The semiconductor chip module as claimed in Claim 15, wherein said first semiconductor chip has a heat dissipating surface that is opposite to said pad mounting surface and that has a heat dissipating plate secured thereon.

18. The semiconductor chip module as claimed in Claim 15, further comprising an encapsulation layer provided on said one of said first and second surfaces of said chip-mounting member to enclose said pad mounting surface of said first semiconductor chip and said first conductor unit.

19. A semiconductor chip module stack, comprising:

upper and lower semiconductor chip modules, each including:

a chip-mounting member having upper and lower surfaces, a set of circuit traces, and a plurality of plated through holes that extend through said upper and lower surfaces and that are connected to said circuit traces,

a semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon,

a dielectric tape member for bonding adhesively said semiconductor chip on said chip-mounting member,

a conductor unit for connecting electrically said contact pads of said semiconductor chip and said circuit traces, and

a plurality of solder balls disposed on said lower surface of said chip-mounting member, each of said solder balls being aligned with and being connected to a respective one of said plated through holes in said chip-mounting member;

wherein said solder balls of said upper semiconductor chip module are aligned with and are connected to said plated through holes in said chip-mounting member of said lower semiconductor chip module at said upper surface of said chip-mounting member of said lower semiconductor chip module.

ABSTRACT OF THE DISCLOSURE

A semiconductor chip module includes a chip-mounting member having opposite first and second surfaces, a set of circuit traces, and a plurality of plated through holes that extend through the first and second surfaces and that are connected to the circuit traces. A dielectric tape member bonds adhesively a semiconductor chip on the chip-mounting member. A first conductor unit connects electrically contact pads on a pad mounting surface of the semiconductor chip and the circuit traces. A plurality of solder balls are disposed on one of the first and second surfaces of the chip-mounting member, are aligned with and are connected to the plated through holes in the chip-mounting member, respectively.

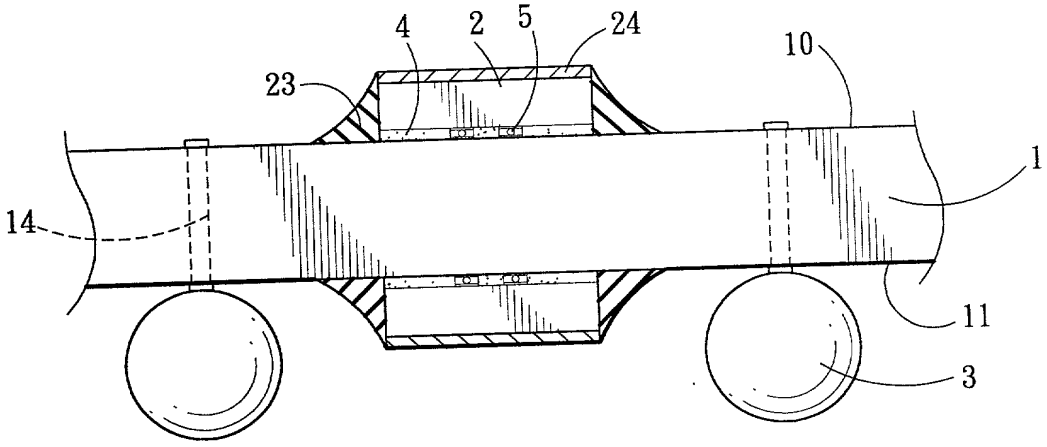

FIG.1

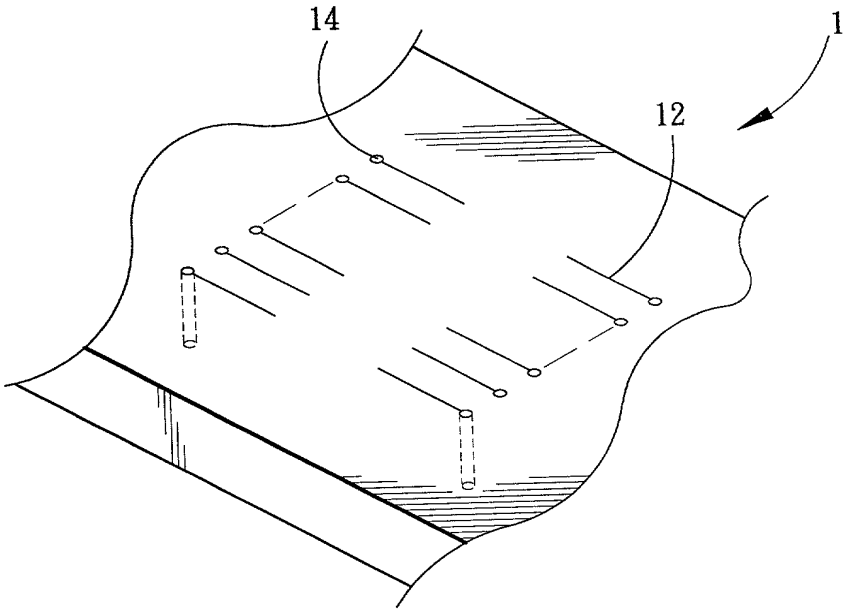

FIG.2

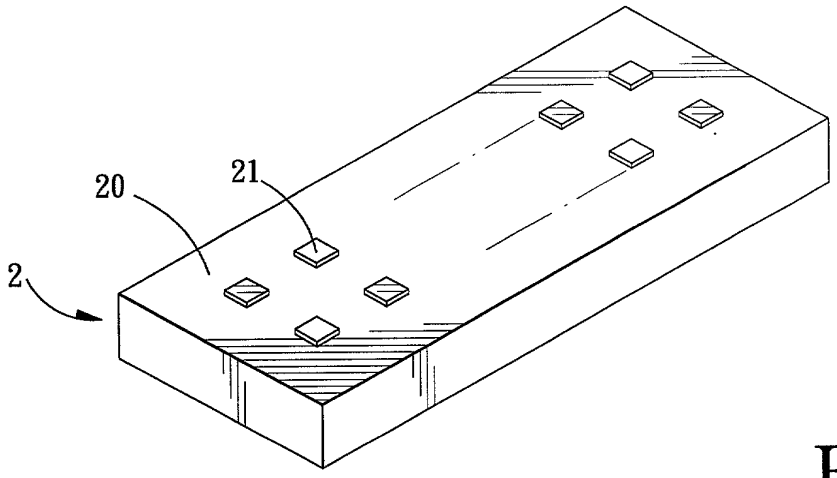

FIG.3

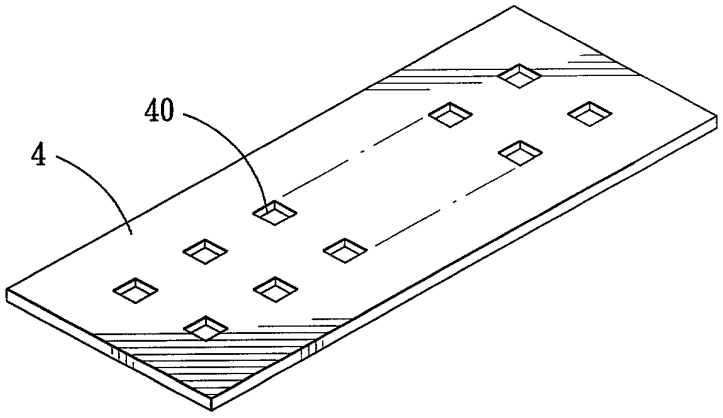

FIG.4

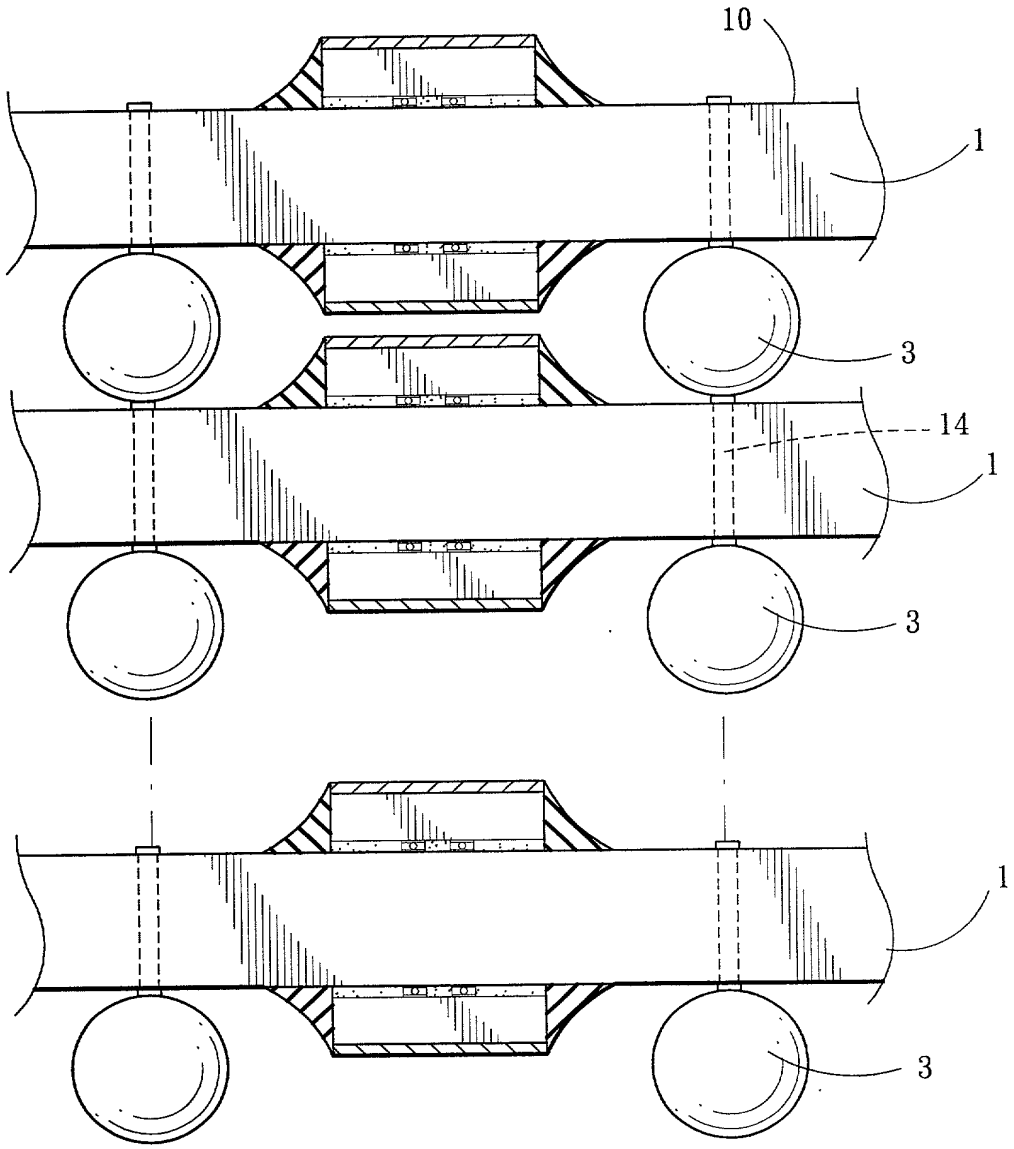

FIG.5

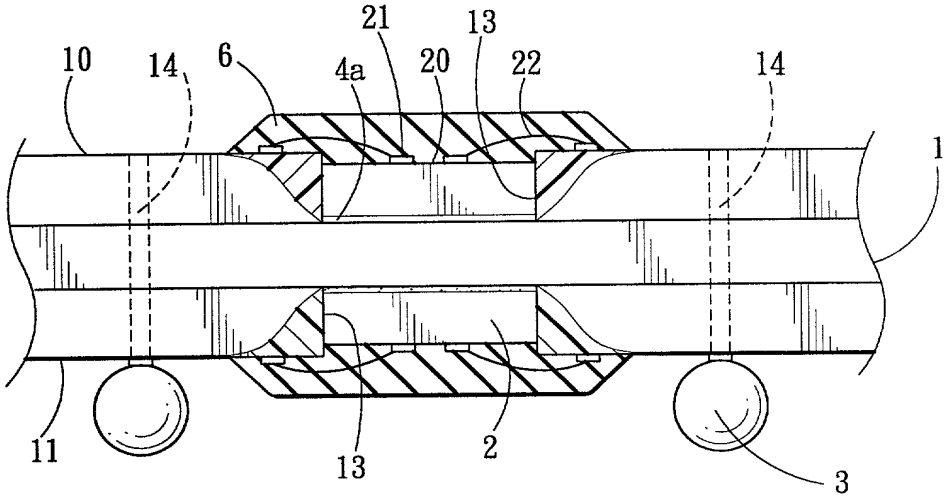

FIG.6

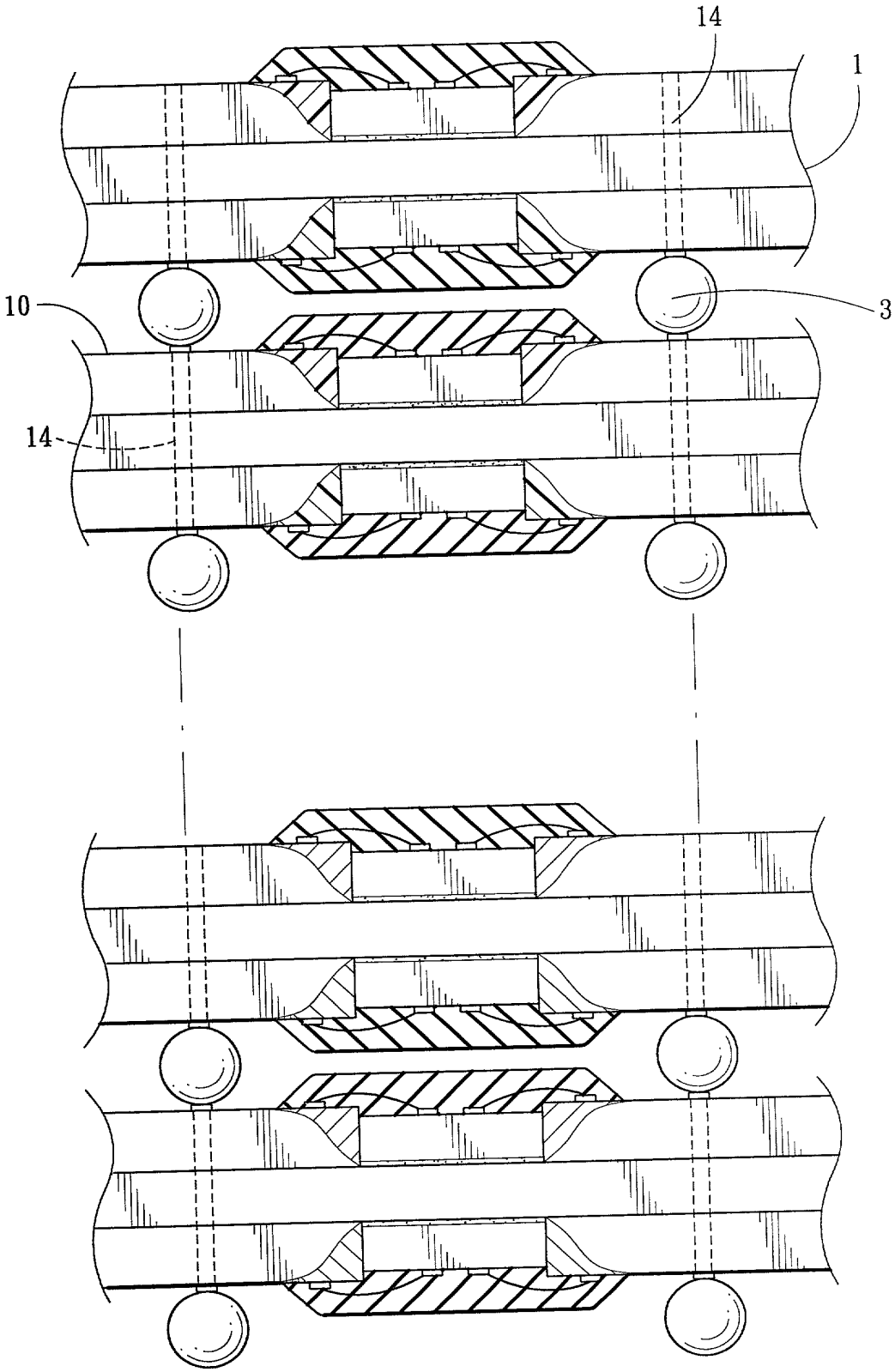

FIG.7

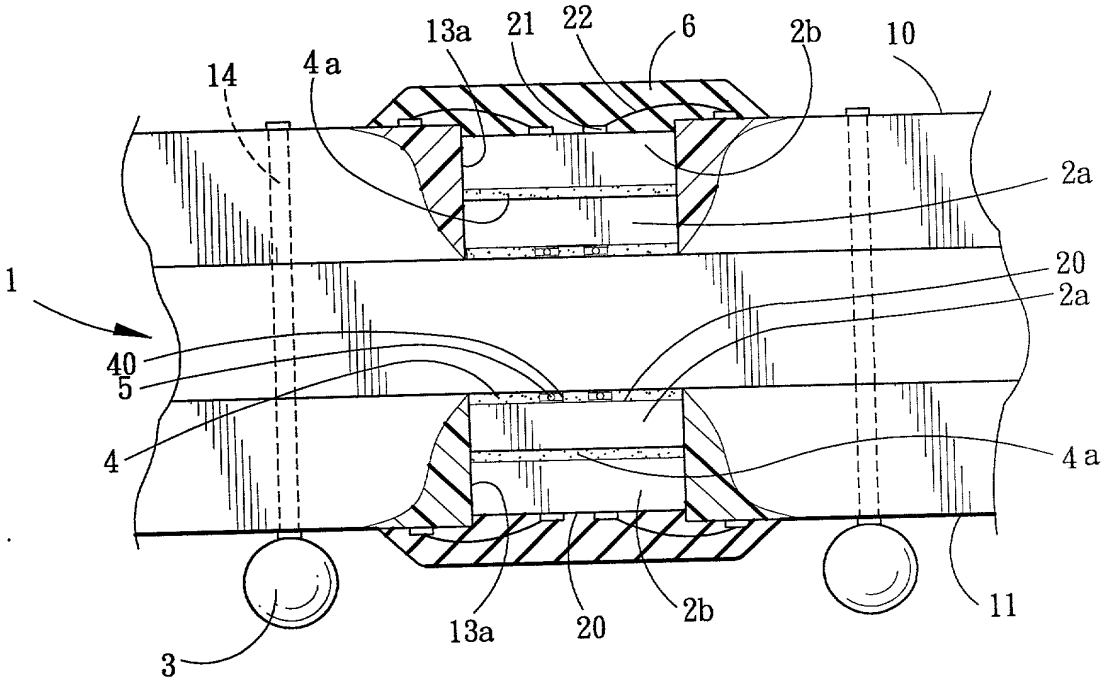

FIG.8

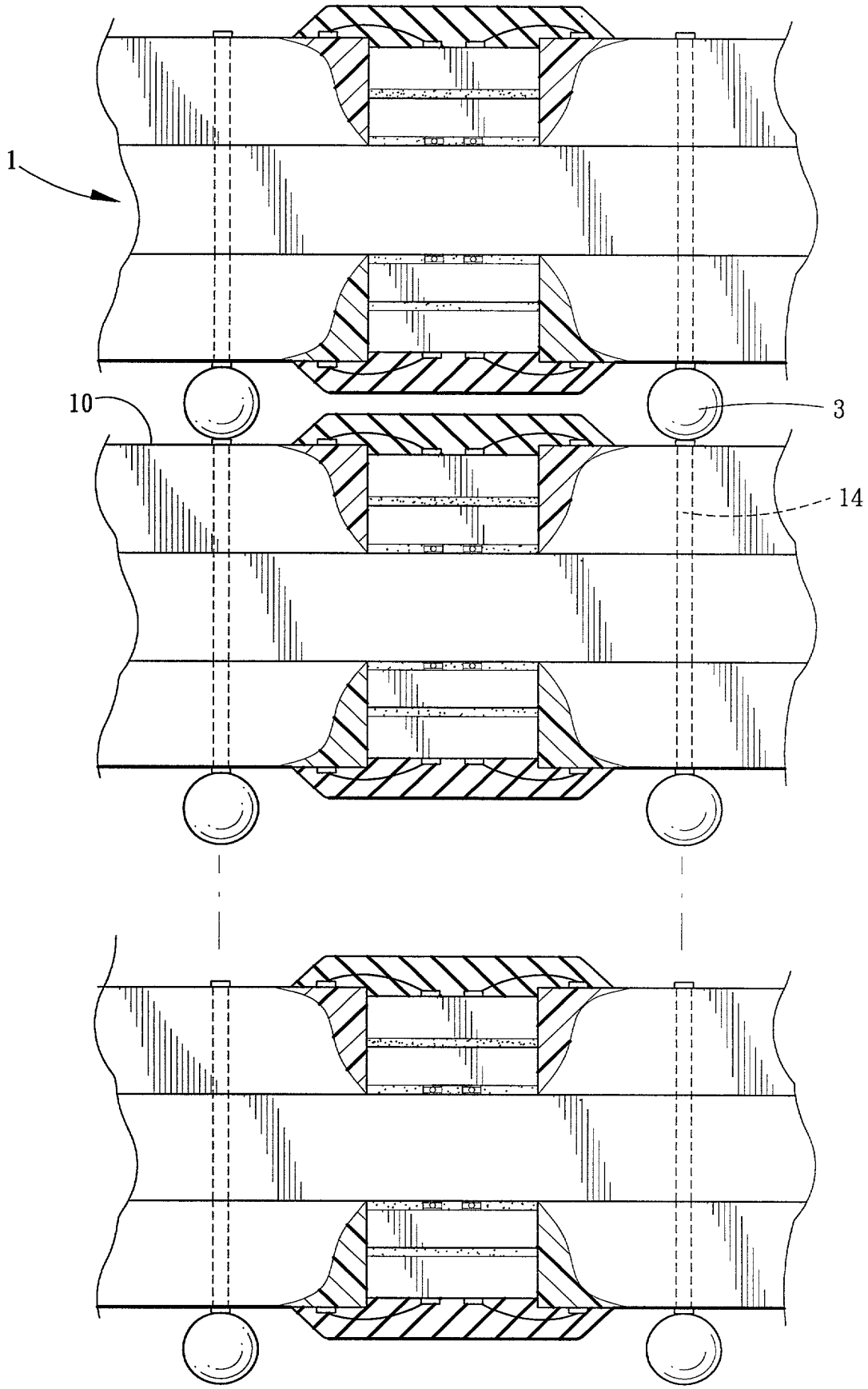

FIG.9

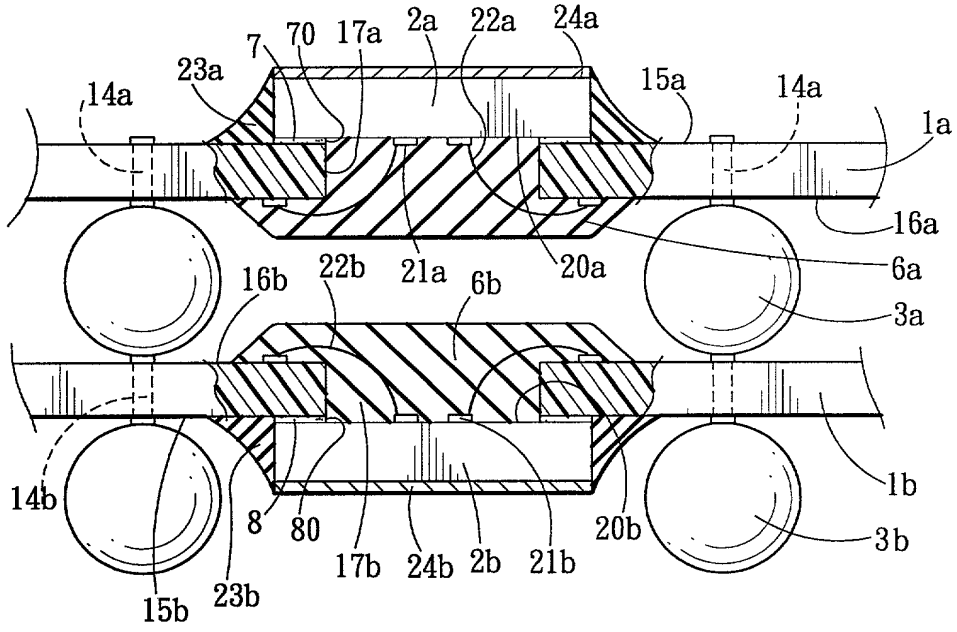
7
70
17a
2a
22a
24a
23a
14a
15a
14a
1a
16a
6a
3a
16b
22b
21a
6b
20a
1b
14b
8
80
17b
24b
2b
21b
20b
3b
15b
23b

FIG.10

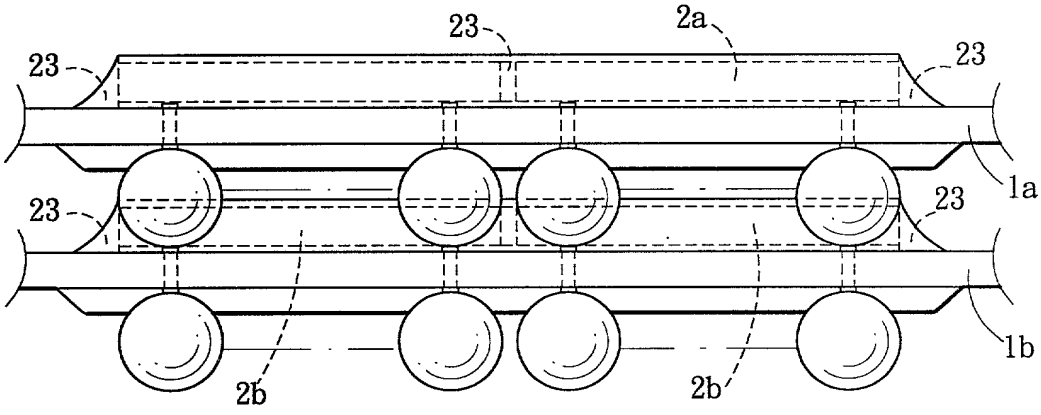
23
2a
23
23
1a
23
23
1b
2b
2b

FIG.12

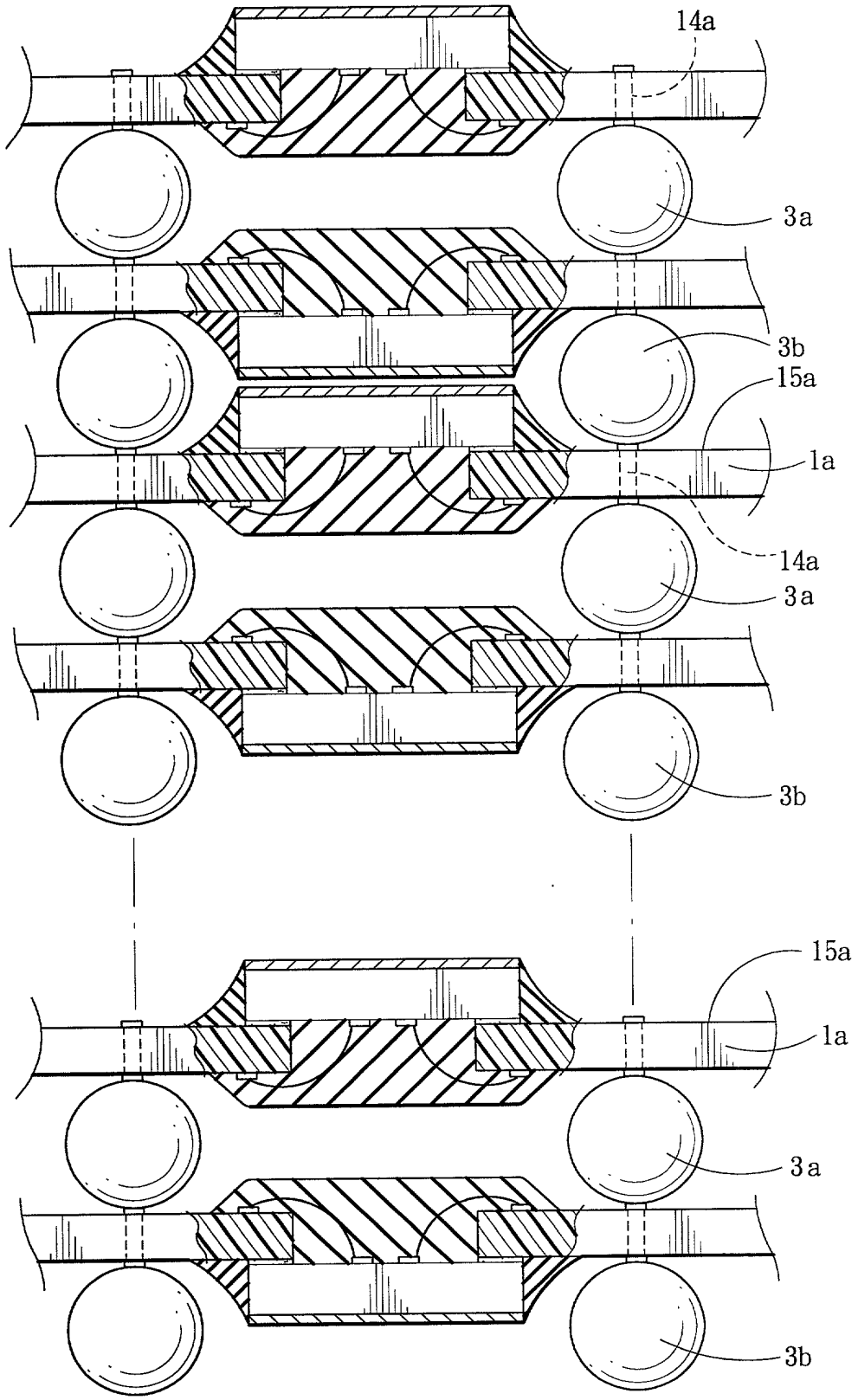

FIG. 11

Declaration and Power of Attorney For Patent Application
專利申請聲明及委托書
Chinese Language Declaration
中文聲明

作爲下述聲明者，我在此宣告：

As a below-named inventor, I hereby declare that:

我的住址、郵局地址和國籍均列在我名下：

My residence, post office address and citizenship are as stated below next to my name,

我相信我是首創的、第一個和唯一的聲明者(如只列出一人姓名)或是首創的、首位共同發明者(如列出數人姓名)。我提出作爲專利申請權利要求的題目如下：

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR CHIP MODULE

如不在下面小方格中打叉則須將說明書附此：

the specification of which is attached hereto unless the following box is checked:

☐ 以美國申請號碼或PCT國際申請號碼_____
立案于_____
修正于(如適用)_____

☐ was filed on _____
as United States Application Number or PCT International Application Number
_____ and was amended on
_____ (if applicable).

我在此聲明我已閱讀並理解上述說明書的內容，包括上述任何修正案所修正的權利要求。

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

按照聯邦法規第三十七節第一．五六條，我有責任提供支持專利權的實質性資料。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations, § 1.56..

Chinese Language Declaration

我申請享受按照美國法規三十五節第一百一十九條列出的以下任何外國專利申請書或發明者証書的外國優先權，並確認下列具有優先權申請前立案日期的、任何外國專利申請書或發明者証書。

I hereby claim foreign priority under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

			是否要求優先權	
88212813	Taiwan	30/July/1999	☒	☐
(號碼) (Number)	(國名) (Country)	(申請日/月/年) (Day/Month/Year Filed)	是 Yes	否 No
			☐	☐
(號碼) (Number)	(國名) (Country)	(申請日/月/年) (Day/Month/Year Filed)	是 Yes	否 No
			☐	☐
(號碼) (Number)	(國名) (Country)	(申請日/月/年) (Day/Month/Year Filed)	是 Yes	否 No

我申請享受按照美國法規第三十五節一百二十條列出的以下任何美國申請書的利益，如果此申請書中提出的每項權利要求的題目未按美國法規第三十五節第一百二十條第一段的要求在以前的美國申請書中披露，則我有責任按照聯邦法規第三十七節第一．五六(甲)條提供支持專利權的實質性資料，這一法規條文生效于以前申請的立案日期之後，但在美國或PCT國際申請立案日期之前。

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(申請順序號碼) (Application Serial No.)	(申請日期) (Filing Date)	(狀況) (已授專利權、申請中、取消)	(Status) (patented, pending, abandoned)
(申請順序號碼) (Application Serial No.)	(申請日期) (Filing Date)	(狀況) (已授專利權、申請中、取消)	(Status) (patented, pending, abandoned)

我在此聲明根據我所知而作的所有聲明都是實無誤，所有有關資料和信息的聲明也是實無誤；我還知道，按照美國法規第十八節第一千零一項，任何蓄意偽造的聲明都將受到罰款或監禁，或同時受到兩種懲罰。這類蓄意偽造的聲明將危及此申請書或任何已頒發專利的效力。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Chinese Language Declaration

委托書：
以列名發明者的身份，我在此指定下列律師和/或代理人執行此申請並從事與專利商標公署有關的所有業務(列出姓名和注冊號碼)：

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agents(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

Please see attachment

回信請寄：

Send Correspondence to:

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90 South Seventh Street
Minneapolis, MN 55402-4131
U.S.A.

直撥電話(姓名及電話號碼)

Direct Telephone Calls to: (name and telephone number)

Attn:Mr. Michael D. Schumann
(612)332-5300

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國籍	Citizenship Taiwan
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	Taipei City, Taiwan
第二個共同發明者全名(如有)	Full name of second joint inventor, if any
第二個發明者簽字 日期	Second Inventor's signature Date
地址	Residence
國籍	Citizenship
郵局地址	Post Office Address

(第三個和其他共同發明者需提供同樣資料和簽字。) (Supply similar information and signature for third and subsequent joint inventors.)

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Beard, John L.	Reg. No. 27,612
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Bejin, Thomas E.	Reg. No. 37,089
Berman, Charles	Reg. No. 29,249
Bogucki, Raymond A.	Reg. No. 17,426
Bruess, Steven C.	Reg. No. 34,130
Byrne, Linda M.	Reg. No. 32,404
Canady, Karen S.	Reg. No. 39,927
Carlson, Alan G.	Reg. No. 25,959
Carter, Charles G.	Reg. No. 35,093
Caspers, Philip P.	Reg. No. 33,227
Chiapetta, James R.	Reg. No. 39,634
Clifford, John A.	Reg. No. 30,247
Conrad, Timothy R.	Reg. No. 30,164
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Dalglish, Leslie E.	Reg. No. P-40,579
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Kastelic, Joseph M.	Reg. No. 37,160
Kettelberger, Denise	Reg. No. 33,924
Komanduri, Janaki	Reg. No. P-40,684
Kowalchyk, Alan W.	Reg. No. 31,535
Kowalchyk, Katherine M.	Reg. No. 36,848
Lacy, Paul E.	Reg. No. 38,946
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McDaniel, Karen D.	Reg. No. 37,674
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McDonald, Wendy M.	Reg. No. 32,427
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Miller, William D.	Reg. No. 37,988
Mueller, Douglas P.	Reg. No. 30,300
Nasiedlak, Tyler L.	Reg. No. 40,099
Nelson, Albin J.	Reg. No. 28,650
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Xu, Min S.	Reg. No. 39,536